AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listing of claims in the application.

1. (Currently Amended) A method of forming at least one dielectrically insulating isolation trench for dielectric isolation of regions of different potential~~, in particular,~~ of device structures formed above an SOI wafer including an active semiconductor layer, by forming at least one void in said at least one isolation trench, thereafter forming a hermetically tight seal of the at least one void with respect to the semiconductor wafer surface, the method comprising:

performing a first fill in the form of a controlled deposition adapted to trench geometry with an aspect ratio of 15 to 1 or higher to thereby form oxide layers at trench walls, said oxide layers having an increasing thickness towards upper trench edges and forming a first bottleneck;

subsequently anisotropically RIE etching the oxide layers in a first step until the oxide layers are removed from the wafer surface and subsequently continuing the RIE etching process in a second step for removing the oxide layers in an upper trench portion to a defined depth for defining a later sealing portion of the at least one void by displacing downwardly the first bottleneck to form a further bottleneck.

2. (Canceled)

3. (Currently Amended) The method according to claim 1 ~~2~~, further comprising a second oxide deposition performed by a low pressure CVD process, thereby again depositing an oxide near a step formed by the further bottleneck to seal the at least one void located therebelow, said second oxide deposition being stopped when the portion of the oxide layer above said at least one void is grown above a wafer level of the semiconductor layer.

4. (Previously presented) The method according to claim 3, wherein after sealing said trench, the wafer surface is planarized and a technological process sequence is continued.

5. (Currently Amended) The method according to claim 1 ~~2~~, wherein the RIE etching of the first trench filling in the area outside said trench stops on a polysilicon layer, which has previously been formed on at least one of a silicon dioxide layer and a multi insulator layer.

6. (Previously presented) The method according to claim 3, wherein the same process technique is used during the first and the second depositions.

7. (Previously presented) The method according to claim 3, wherein different process techniques are used during the first and the second depositions.

8. (Previously presented) The method according to claim 1, wherein said SOI wafer comprises micro electronic mechanic systems (MEMS) in a semiconductor layer formed on the oxide layer.

9. (Canceled).

10. (Previously presented) The method according to claim 3, wherein the formed sealed of the at least one void is located below the level of the surface of the active semiconductor layer.

11. (Previously presented) The method according to claim 1, wherein a surface of the sealed trench is planarized.

12. (Canceled)

13. (Withdrawn) A processed SOI wafer comprising at least one insulation trench having a sealed void, an upper end of said sealed void ending below a surface of an active semiconductor layer of the SOI wafer, said SOI wafer formed by a process comprising the steps of:

performing a first fill in the form of a controlled deposition adapted to trench geometry thereby forming oxide layers at trench walls, said oxide layers having an increasing thickness towards upper trench edges and forming a first bottleneck;

etching the oxide layers in a first step until the oxide layers are removed from the wafer surface; and

continuing the etching process in a second step for removing the oxide layer in an upper trench portion to a defined depth for at least one of defining a later sealing portion of the sealed void and displacing downwardly the first bottleneck to form a further bottleneck; and

performing a second fill in the form of a controlled deposition thereby again depositing an oxide near at least one of a step formed previously and the further bottleneck, thereby resulting in sealing the sealed void located therebelow, said second fill being stopped when the sealed portion of the oxide layer above the sealed void is grown above a wafer level of the semiconductor layer.

14. (Withdrawn) The SOI wafer according to claim 13, wherein a notch tip extending downwardly and located above said sealed void terminates above horizontal level of the surface of the active semiconductor layer.

15. (Withdrawn) A method for filling isolation trenches having a high aspect ratio for dielectrically isolating regions of different potentials of device structures formed on an SOI wafer by forming, based on the insulator filling of the respective trench, a void having a hermetically tight sealing below a level of the semiconductor wafer surface, and by planarizing subsequent to the filling of the trench having the maintained void and by performing a sequence of CMOS process steps after forming said trench comprising:

forming SiO_2 layers by a first CVD process, said SiO_2 layers having a thickness increasing towards the upper trench edges;

completely removing SiO_2 portions at the upper trench portion to a defined depth so as to determine a later sealing point of the void, by a substantially anisotropic etch process, thereby creating a step at a narrowest portion in the trench; and

sealing a respective void and filling the respect said trench by depositing a second SiO_2 layer by a second low pressure CVD process such that a tip of a notch of the formed second SiO_2 layer is positioned above the level of the semiconductor wafer surface.

16. (Withdrawn) The method according to claim 15, wherein said step of completely removing SiO_2 portions at the upper trench portion to a defined depth so as to determine a later sealing

point of the void terminates in the region outside said trench at a polysilicon layer formed on at least one SIO_2 layer.

17. (Withdrawn) The method according to claim 15, wherein the same process technique is used in the first and second CVD processes.

18. (Withdrawn) The method according to claim 15, wherein different process techniques are used in the first and second CVD processes.

19. (Withdrawn) The method according to claim 15, wherein said SOI wafer comprises microelectronic mechanic systems (MEMS) in a semiconductor layer formed above the oxide layer.